WHAT IS CLAIMED IS:

1. Branch prediction circuitry comprising:

a bimodal branch history table comprising a plurality of entries each for storing a prediction value and accessed by selected bits of a branch address;

a fetch-based branch history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of said branch address and bits from a history register; and

a selector table comprising a plurality of entries each for storing a selection bit and accessed by a pointer generated from selected bits from said branch address and bits from said history register, each said selector bit used for selecting between a bimodal prediction value accessed from the bimodal history table and a prediction value accessed from said fetch-based history table.

2. The branch prediction circuitry of Claim 1 and further comprising circuitry for updating said bimodal and fetch-based branch history tables operable to:

set a corresponding entry in each of said bimodal and fetch-based branch history tables when a branch is taken at branch resolution time; and

set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time.

3. The branch prediction circuitry of Claim 1 and further comprising circuitry for updating said selector table operable to:

update a selected entry in said selector table with a first value when a bimodal prediction value from said bimodal branch history table correctly represents a corresponding branch resolution; and

update a selected entry in said selector table with a second value when a fetch-based prediction value from said fetch-based branch history table correctly represents the corresponding branch resolution.

4. The branch prediction circuitry of Claim 3 wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when corresponding values from said bimodal and fetch based branch history tables both correctly represent a corresponding branch resolution.

5. The branch prediction circuitry of Claim 3 wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when neither values from said bimodal and fetch-based branch history tables correctly represent a corresponding branch resolution.

6. The branch prediction circuitry of Claim 3 wherein said circuitry for updating said selector table is further operable to set a value in a selected entry in said selector table to a value associated with said fetch-based table when corresponding values from said bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome.

7. The processing system of Claim 1 wherein said history register comprises a shift register and said branch prediction circuitry further comprises circuitry for updating said shift register by shifting in a preselected value in response to a prediction value from a selected one of said branch history tables as selected in response to a corresponding said selector bit.

8. A processing system comprising:

a first branch history table comprising a plurality of bimodally accessed entries for storing a first set of branch prediction bits;

a second branch history table comprising a plurality of fetch-based accessed entries for storing a second set of branch prediction bits;

a selector for selecting in response to a selection control bit selected from a set of selection control bits, a bit from a selected one of said sets of bits accessed from said first and second branch history tables; and

a selector table comprising a plurality of entries for storing said a set of selector bits as a function of a performance history of said first and second sets of branch prediction bits stored in said first and second branch history tables.

9. The processing system of Claim 8 wherein said entries of said selector table are accessed using fetch-based accessing.

10. The processing system of Claim 8 wherein said each said entry in said tables comprises a 1-bit counter.

11. The processing system of Claim 8 wherein said first and second branch history tables and said selector table form a portion of a branch execution unit.

12. The processing system of Claim 11 wherein said branch execution unit forms a part of a microprocessor.

13. The processing system of Claim 12 and further comprising memory coupled to said microprocessor.

14. A method of performing branch predictions in a processing system including a bimodal branch history table, a fetch-based branch history table and a selector table, the method comprising the substeps of:

accessing the bimodal branch history table to retrieve a first branch prediction bit;

accessing the fetch-based branch history table to retrieve a second branch prediction bit;

selecting between the first and second branch prediction bits in response to a bit retrieved from the selector table; and

updating the selector table as a function of actual branch resolution.

15. The method of Claim 14 wherein said step of updating the selector table comprises the substeps of:

determining if the first branch prediction bit correctly predicts the branch resolution outcome;

updating the corresponding entry in the selector table to a first logic value when the first prediction bit correctly represents the branch resolution outcome;

determining if the second branch prediction bit correctly predicts the branch resolution outcome; and

updating the corresponding entry in the selector table to a second logic value when the second branch prediction bit correctly represents the branch resolution outcome.

16. The method of Claim 15 and further comprising the steps of:

determining if both the first and second branch history bits correctly predict the branch resolution outcome;

maintaining the current value in the corresponding selector table entry when both the first and second branch prediction bits correctly predict the branch resolution outcome;

determining if both the first and second branch prediction bits incorrectly predict the branch resolution outcome; and

maintaining the current value in the corresponding selector table entry when both the first and second branch history bits incorrectly predict the branch history outcome.

17. The method of Claim 15 and further comprising the steps of:

determining whether both the first and second branch prediction bits correctly predict the branch resolution outcome;

maintaining the current value in the corresponding selector table entry when both the first and second branch prediction bits correctly predict the branch resolution outcome; and

updating the current selector table entry to a logic value associated with the fetch-based branch history table when neither the first nor second branch prediction bits correctly predicts the branch resolution outcome.

18. The method of Claim 14 wherein said step of accessing the fetch-based branch history table comprises the substep of generating an address from at least some bits of a branching instruction and bits retrieved from a history register.

19. The method of Clam 18 wherein the history register comprises a shift register.

20. The method of Claim 19 wherein said method further comprises the steps of updating the shift register by shifting-in the prediction bit selected by said step of selecting.

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